INSTITUTE OF TECHNOLOGY
& MANAGEMENT
GWALIOR • MP • INDIA

Laboratory Manual

DCS
(IT-305)

For

Second Year Students

Department: Information Technology

Department of Information Technology

Vision of IT Department

The Department of Information Technology envisions preparing technically competent problem solvers, researchers, innovators, entrepreneurs, and skilled IT professionals for the development of rural and backward areas of the country for the modern computing challenges.

Mission of the IT Department

- To offer valuable education through an effective pedagogical teaching-learning process.
- To shape technologically strong students for industry, research & higher studies.
- To stimulate the young brain entrenched with ethical values and professional behaviors for the progress of society.

Program Educational Objectives

Graduates will be able to

- Our graduates will show management skills and teamwork to attain employers' objectives in their careers.
- Our graduates will explore the opportunities to succeed in research and/or higher studies.
- Our graduates will apply technical knowledge of Information Technology for innovation and entrepreneurship.
- Our graduates will evolve ethical and professional practices for the betterment of society.

Program Outcome (POs)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering Fundamentals, and an engineering specialization to the solution of complex engineeringproblems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problemsand design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, andenvironmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data,and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilitiesand norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member orleader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, andgive and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of theengineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Course Outcomes

DCS (IT-305)

CO1:	Student will be able to understand and apply the basic concept digital electronics for digital circuit and system design.
CO2:	Students will be able to realize and describe the operation of combinational circuits.
CO3:	Students will be able to realize and describe the operation of sequential circuits
CO4:	Students will be able to apply the fundamental knowledge of digital electronics principle for understanding and creating different (unipolar and boipolar) logic families.
CO5:	Students will be able to apply the fundamental knowledge of analog and digital electronics principle for understanding and creating different analog to digital converter, multi-vibrator

Course	P01	P02	P03	P04	P05	P06	P07	P08	P09	P010	P011	P012	PSO1	PSO2	PSO3
CO1	2	1	0	1	0	0	0	0	0	0	0	0	0	0	0
CO2	1	2	1	1	0	0	0	0	0	0	0	0	0	0	0
CO3	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
CO4	1	1	0	0	0	0	0	0	0	0	0	0	2	0	1
CO5	1	1	0	0	0	0	0	0	0	0	0	0	2	0	0
Avg	**1.2**	**1.2**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

List Of Experiment

1. Verification of Different Basic Digital Logic Gates for Various Ic's.

NAME OF LABORATORY: Digital System Design Lab
LAB SUBJECT NAME/CODE: DCS / IT-305 NAME OF DEPARTMENT: - E.C

Date of conduction: -

Date of submission: -

Submitted by other members: -

1. 2.

3. 4.

5. 6.

7. 8.

Group no: -

Signature

Name of faculty in charge:

Name of Technical Assistant:

OBJECT: - To Test and operation of different basic digital logic Gates for various IC's and verification of their Truth Table.

APPARATUS REQUIRED:

S.No.	COMPONET	SPECIFICATION	QTY
	AND GATE	IC 74081	
	OR GATE	IC 7432	
	NOT GATE	IC 7404	
	NAND GATE 2 I/P	IC 7400	
	NOR GATE	IC 7402	
	X-OR GATE	IC 7486	
	IC TRAINER KIT	-	
	WIRES	-	As Required

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.OR, AND and NOT are basic gates. NAND, NOR and X-OR are known as universal gates.Basic gates form these gates**.**

AND GATE:

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR GATE:

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT GATE:

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

NAND GATE:

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low.The output is low level when both inputs are high.

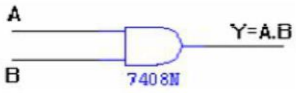
NOR GATE:

The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

X-OR GATE:

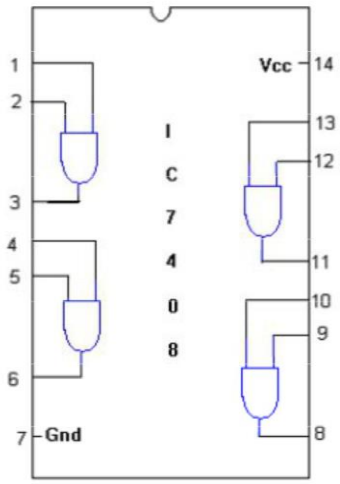
The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

AND GATE:PIN DIAGRAM



TRUTH TABLE

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1



OR GATE :

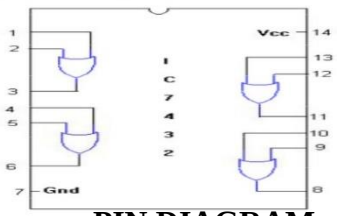
SYMBOL :

TRUTH TABLE

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE

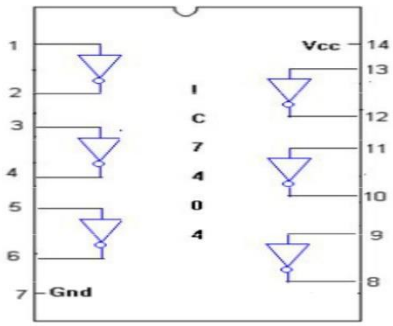
PIN DIAGRAM :



PIN DIAGRAM

TRUTH TABLE :

A	$\overline{A}$
0	1
1	0

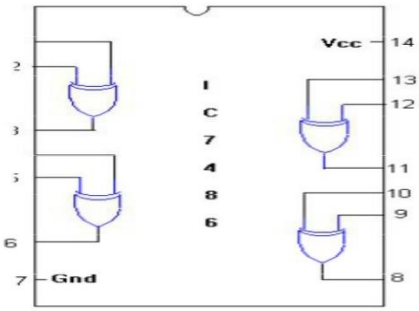


X-OR GATE :

PIN DIAGRAM

TRUTH TABLE :

A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

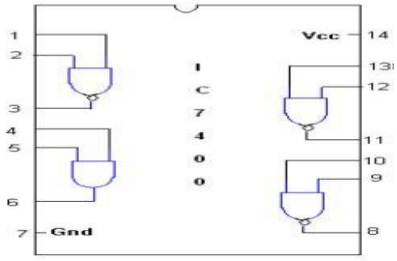


2-INPUT NAND GATE:

PIN DIAGRA

TRUTH TABLE

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0



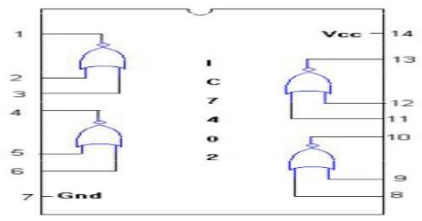
NOR GATE:

SYMBOL :

TRUTH TABLE

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

PIN DIAGRAM:



PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board.
3. Connect the inputs to the input switches provided in the Bread board.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions of LEDs.
6. Similarly follow these steps for other gates.

PRECAUTIONS:

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.
5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
6. Take care while removing and inserting the IC on bread board.

RESULT:

Thus the logic gates are studied and their truth tables were verified.

2. Implement of AND, OR, NOT, Gates by NAND and NOR Universal gates.

NAME OF LABORATORY: Digital System Design Lab
LAB SUBJECT NAME/CODE: DCS/ IT-305
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Date of submission: -

Submitted by other members: -

1. 2.

3. 4.

5. 6.

7. 8.

Group no: -

Signature

Name of faculty in charge:

Name of Technical Assistant:

OBJECT:- Implementation Of AND, OR, NOT, Gates By NAND And NOR

Universal Gates

APPARATUS REQUIRED: - TRAINER KIT (OR)

S.No.	COMPONET	SPECIFICATION	QTY

1.	NAND GATE	IC 7400	
2.	NOR GATE	IC 7402	
3.	BREAD BOARD	WHITE COLOR	
4.	SLIDE SWITCH	ON/OFF TYPE	
5.	LED	ANY COLOR	
6.	RESISTANCE	10,100 Ohm	
7.	+5v.DC Power	-	
8.	JUMPER WIRES	-	As Required

THEORY:

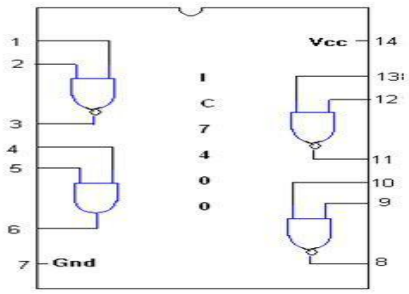
NAND GATE:

The NAND gate is a Universal Gate by the use of this gate we can implement all other gates. The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low .The output is low level when both inputs are high.

2-INPUT NAND GATE:

TRUTH TABLE

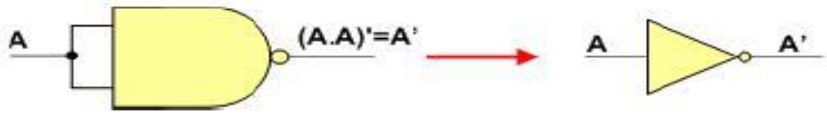
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0



Implementing an Inverter Using only NAND Gate:

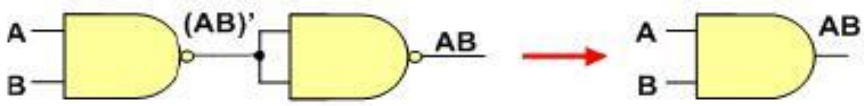
The figure shows two ways in which a NAND gate can be used as an inverter (NOT gate).

All NAND input pins connect to the input signal A gives an output A'.



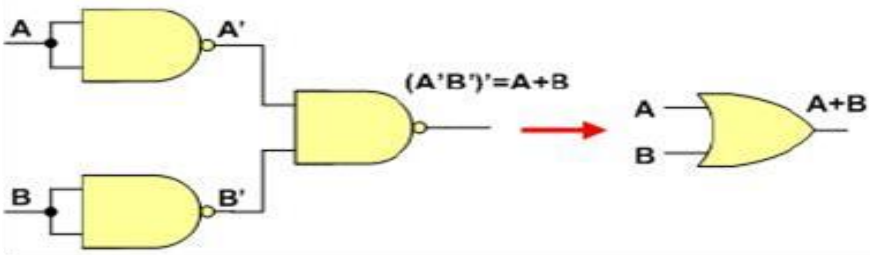
Implementing AND Using only NAND Gates

An AND gate can be replaced by NAND gates as shown in the figure (The AND is replaced by a NAND gate with its output complemented by a NAND gate inverter).



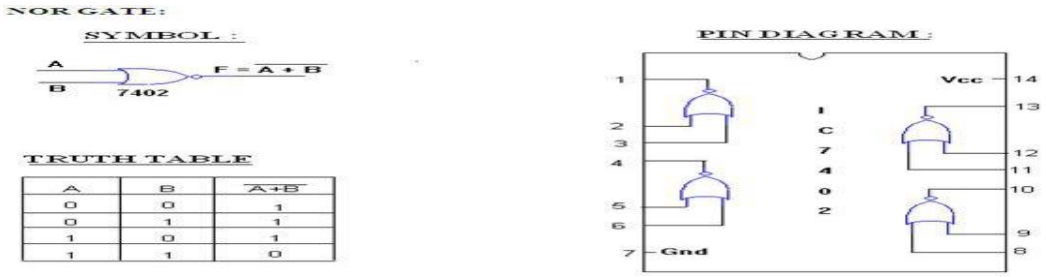
Implementing OR Using only NAND Gates

An OR gate can be replaced by NAND gates as shown in the figure (The OR gate is replaced by a NAND gate with all its inputs complemented by NAND gate inverters).



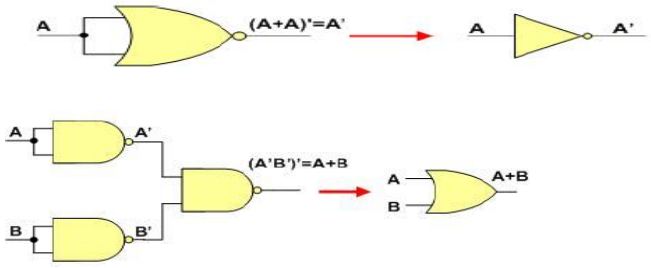
NOR GATE:

The NOR gate is a Universal Gate by the use of this gate we can implement all other gates The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are hi



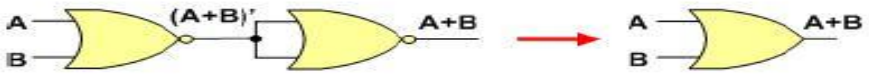
Implementing an Inverter Using only NOR Gate

The figure shows two ways in which a NOR gate can be used as an inverter (NOT gate).AllNOR input pins connect to the input signal A gives an output A'.



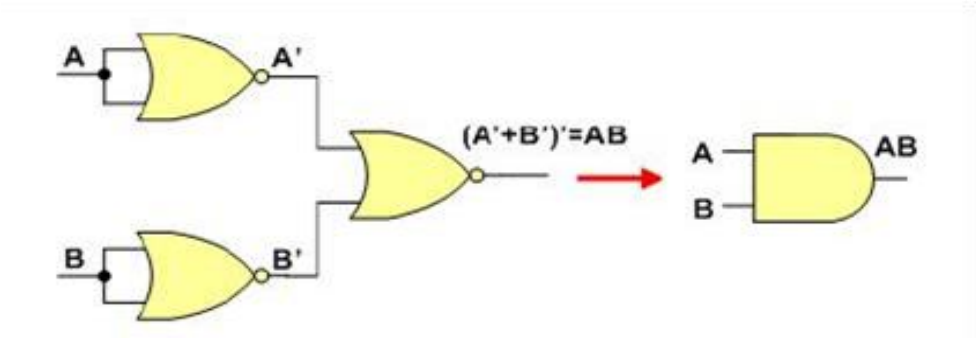
Implementing OR Using only NOR Gates

An OR gate can be replaced by NOR gates as shown in the figure (The OR is replaced by a NOR gate with its output complemented by a NOR gate inverter)



Implementing AND Using only NOR Gates

An AND gate can be replaced by NOR gates as shown in the figure (The AND gate is replaced by a NOR gate with all its inputs complemented by NOR gate inverters).



PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board.
3. Connect the inputs to the input switches provided in the Bread board.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions of LEDs.
6. Similarly follow these steps for other gates.

PRECAUTIONS:

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.
5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
6. Take care while removing and inserting the IC on bread board.

RESULT:

Thus the logic gates are studied and their truth tables were verified.

2(B). Verification of versatility of NAND gate and NOR gate

NAME OF LABORATORY: Digital System Design Lab
LAB SUBJECT NAME/CODE: DCS / IT-305
NAME OF DEPARTMENT: - E.C.

Date of conduction: -

Date of submission: -

Submitted by other members: -

1. 2.

3. 4.

5. 6.

7. 8.

Group no: -

Signature

Name of faculty in charge:

Name of Technical Assistant:

OBJECT:- (i)Implementation Of NOR GATE, EX-OR, Gates using by NAND Universal Gates.

(ii) Implementation Of NAND GATE, EX-OR, Gates using by NOR Universal Gates.

APPARATUS REQUIRED: - TRAINER KIT (or)

S.No.	COMPONET	SPECIFICATION	QTY
	NAND GATE	IC 7400	
	NOR GATE	IC 7402	
	BREAD BOARD	WHITE COLOR	
	SLIDE SWITCH	ON/OFF TYPE	
	LED	ANY COLOR	
	RESISTANCE	10,100 Ohm	
	+5v.DC Power	-	
	JUMPER WIRES	-	As Required

THEORY:

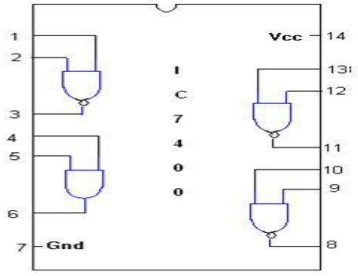
NAND GATE:

The NAND gate is a Universal Gate by the use of this gate we can implement all other gates. The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low .The output is low level when both inputs are high.

2-INPUT NAND GATE:

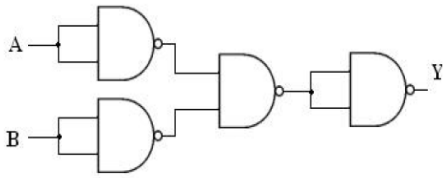
TRUTH TABLE

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0



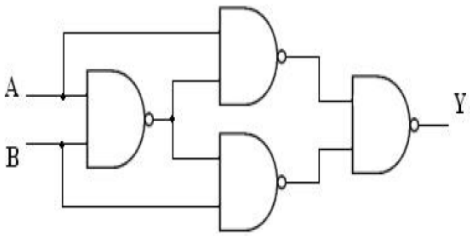
CIRCUIT DIAGRAM WITH TRUTH TABLE:

Implementing of NOR GATE Using by Universal NAND Gate:



2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

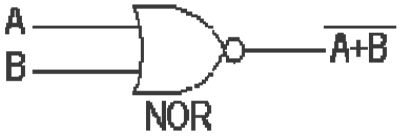
Implementing of EX-OR GATE Using by Universal NAND Gates



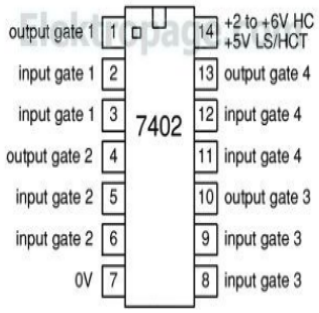
2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

Theory:

NOR gate: OR followed by inverter. It is also known as universal gate. The symbolic representation is:



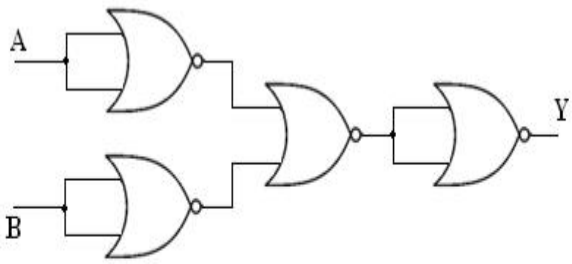
2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion. NOR gate is important gate because NOR considered universal gates. Construct all of the other basic gates using only NOR gate.

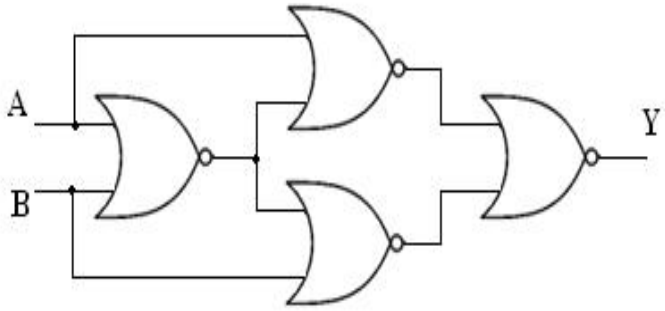
A Truth Table defines how a gate will react to all possible input combinations.

Implementing of NAND GATE Using by Universal NOR Gates



2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

Implementing of EX-NOR GATE Using by NOR Gates



2 Input EXOR gate		
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board.
3. Connect the inputs to the input switches provided in the Bread board.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions LEDs.
6. Similarly follow these steps for other gates.

PRECAUTIONS:

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.
5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
6. Take care while removing and inserting the IC on bread board.

RESULT:

Thus the logic gates are studied and their truth tables were verified.

3. TO PROVE THE DIFFERENT BOOLEAN LAWS

NAME OF LABORATORY: Digital System Design Lab
LAB SUBJECT NAME/CODE: DCS / IT-305NAME OF DEPARTMENT: - E.C

Date of conduction: -

Date of submission: -

Submitted by other members: -

1.	2.
3.	4.
5.	6.
7.	8.

Group no: -

Signature

Name of faculty in charge:

Name of Technical Assistant

OBJECT: - Boolean algebra uses many of the same laws as those of ordinary algebra.

In this experiment, we'll know about these laws.

APPARATUS REQUIRED: -

S.No.	COMPONET	SPECIFICATION	QTY
	AND GATE	IC 74081	
	OR GATE	IC 7432	
	NOT GATE	IC 7404	
	NAND GATE 2 I/P	IC 7400	
	NOR GATE	IC 7402	
	X-OR GATE	IC 7486	
	IC TRAINER KIT	-	
	WIRES	-	As Required

THEORY:

Generally, you'll find that the basic logic functions AND, OR, NAND, NOR, and NOT are not sufficient to implement complex digital logic functions. These gates are the basis for building more complex logic circuits that are constructed using various combinations of gates which is known as Combinational Logic. Combinational logic requires the use of two or more gates to form a useful, complex function. These complex functions usually Begin as a Boolean Equation and the logic circuit may be implemented directly from this Equation. The Boolean laws and rules are shown below:

Laws:

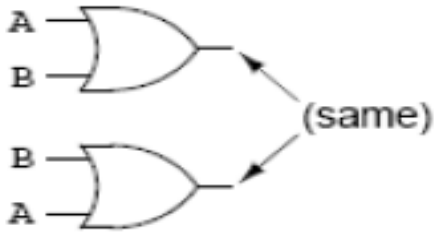
Commutative property of addition:

A + B = B + A

O/P Y1=A+B

O/P Y2=B+A

O/P Y1=A+B



O/P Y2=B+A

FIG: 12.1. Commutative property of addition

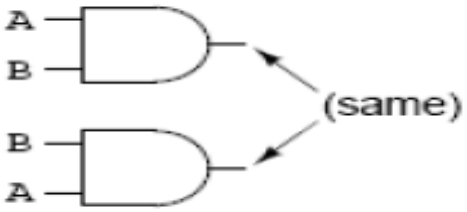
Commutative property of multiplication :

A. B = B. A

O/P Y=A.B

O/P Y=B.A

O/P Y=A.B



O/P Y=B.A

FIG: 12.2. Commutative property of multiplication

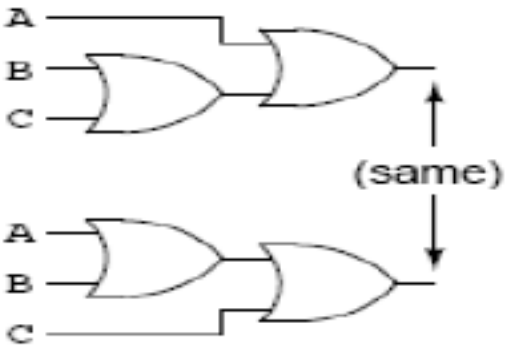
Associative property of addition :

A + (B + C) = (A + B) + C

O/P Y= A + (B + C)

O/P Y= (A + B) + C

O/P Y= A + (B + C)



O/P Y= (A + B) + C

FIG: 12.3. Associative property of addition

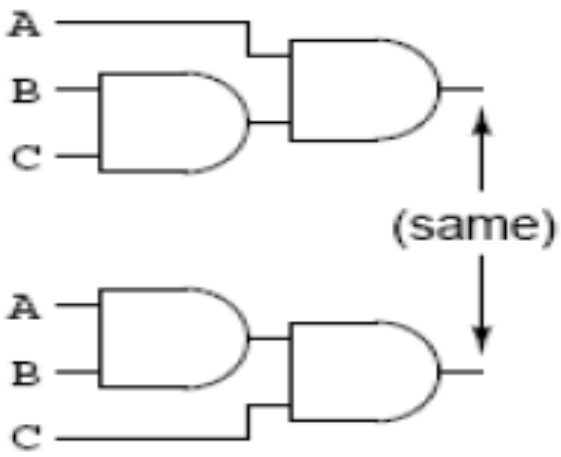
Associative property of multiplication:

A. (B. C) = (A. B). C

O/P Y= A. (B. C)

O/P Y= (A. B). C

O/P Y= A. (B. C)



O/P Y= (A. B). C

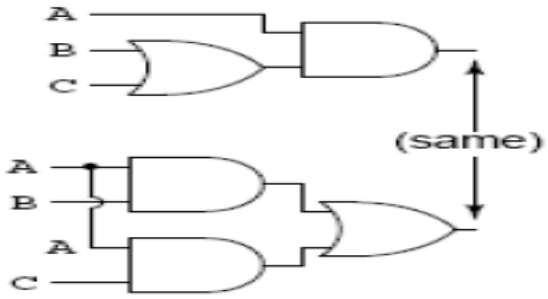
FIG: 12.4. Associative property of multiplication

Distributive property :

A. (B + C) = A. B + A. C

O/P Y= A. (B + C)

O/P Y= A. B + A. C O/P Y= A. (B + C)



O/P Y= A. B + A. C

FIG: 12.5. Distributive propert

PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board.
3. Connect the inputs to the input switches provided in the Bread board.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions of LEDs.
6. Similarly follow these steps for other gates.

PRECAUTIONS:

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.
5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

6. Take care while removing and inserting the IC on bread board.

RESULT:

Thus the logic gates are studied and their truth tables were verified.

4. Verification of various Half Adder and Full Adder circuit by Binary Addition.

NAME OF LABORATORY: Digital System Lab
LAB SUBJECT NAME/CODE: DCS /IT-305NAME OF DEPARTMENT: - E.C

Date of conduction: -

Date of submission: -

Submitted by other members: -

1.	2.
3.	4.
5.	6.
7.	8.

Group no: -

Signature

Name of faculty in charge:

Name of Technical Assistant:

OBJECT:-Verification of various Half Adder and Full Adder circuit by Binary Addition.

APPARATUS REQUIRED: -

S.No.	COMPONET	SPECIFICATION	QTY
	AND GATE	IC 74081	
	OR GATE	IC 7432	
	NOT GATE	IC 7404	
	EX-OR GATE	IC 7486	
	IC TRAINER KIT	-	
	WIRES	As Required	

THEORY:

HALF ADDER:

A half adder has two inputs for the two bits to be added and two outputs one from the sum ‘ S’ and other from the carry ‘ c’ into the higher adder position. Above circuit is called as a carry signal from the addition of the less significant bits sum from the X-OR Gate the carry out from the AND gate.

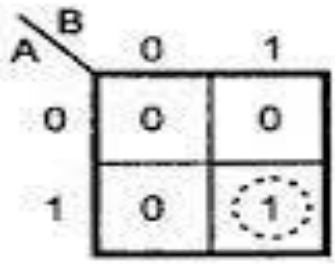
FULL ADDER:

A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs and two outputs. A full adder is useful to add three bits at a time but a half adder cannot do so. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate.

HALF ADDER TRUTH TABLE:

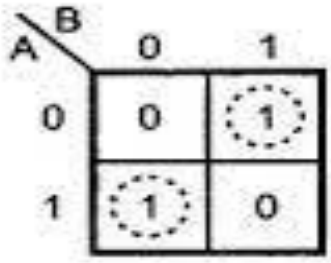
A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

For Carry



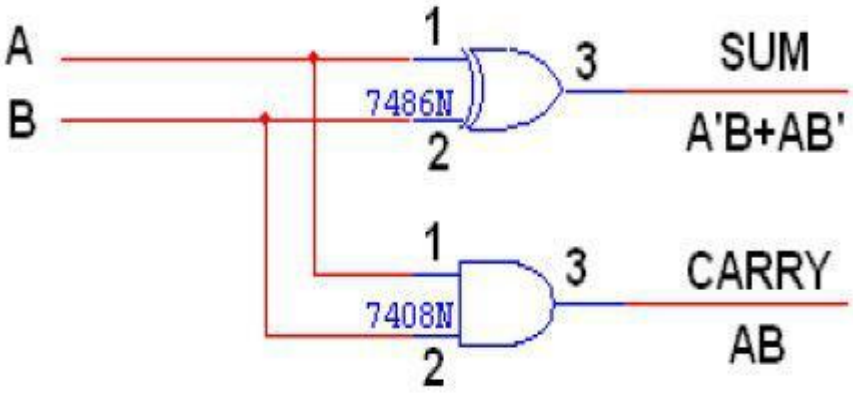
Carry = AB

For Sum



Sum = $A\overline{B} + \overline{A}B$
= $A \oplus B$

LOGIC DIAGRAM:



FULL ADDER TRUTH TABLE

A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

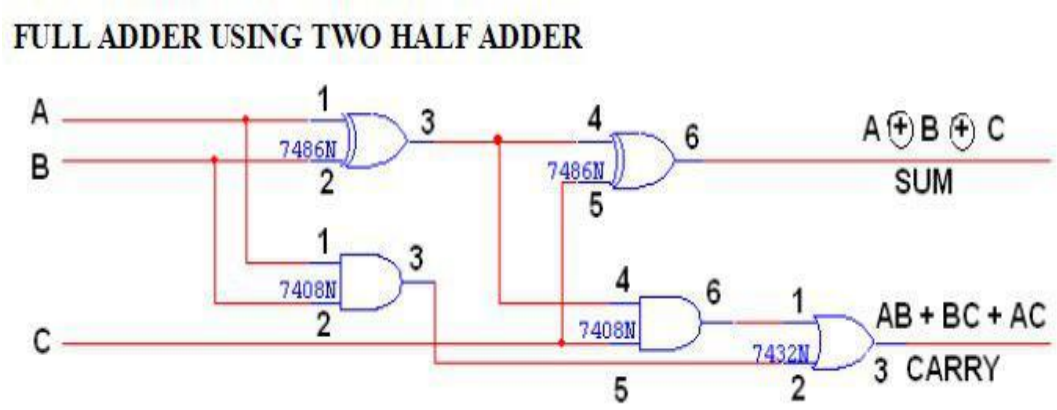
K-Map for SUM:

A \ BC	00	01	11	10
0		1		1
1	1		1	

SUM = A'B'C + A'BC' + ABC' + ABC

K-Map for CARRY:

LOGIC DIAGRAM:



PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board.
3. Connect the inputs to the input switches provided in the Bread board.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions of LEDs.
6. Similarly follow these steps for other gates

PRECAUTIONS:

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.
5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
6. Take care while removing and inserting the IC on bread board.

RESULT:

Thus the half adder and full adder was designed and their truth table is verified.

5. Binary Subtraction by Half Subtractor and Full Subtractor circuit.

NAME OF LABORATORY: Digital System Lab
LAB SUBJECT NAME/CODE: DCS /IT-305NAME OF DEPARTMENT: - E.C

Date of conduction: -

Date of submission: -

Submitted by other members: -

1. 2.

3. 4.

5. 6.

7. 8.

Group no: -

Signature

Name of faculty in charge:

Name of Technical Assistant:

OBJECT:-To design and construct Half Subtractor and Full Subtractor circuits and Verify their truth table using logic gates.

APPARATUS REQUIRED: -

S.No.	COMPONET	SPECIFICATION	QTY
	AND GATE	IC 74081	
	OR GATE	IC 7432	
	NOT GATE	IC 7404	
	EX-OR GATE	IC 7486	
	IC TRAINER KIT	-	
	WIRES	As Required	

THEORY:

HALF SUBTRACTOR:

The half subtractor is constructed using X-OR and AND Gate. The half subtractor has two input and two outputs. The outputs are difference and borrow. The difference can be applied using X-OR Gate, borrow output can be implemented using an AND Gate and an inverter

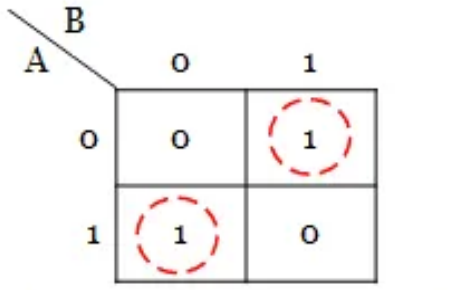
FULL SUBTRACTOR:

The full subtractor is a combination of X-OR, AND, OR, NOT Gates. In a full subtractor the logic circuit should have three inputs and two outputs. The two half subtractor put together gives a full subtractor.The first half subtractor will be C and A B. The output will be difference output of full subtractor. The expression AB assembles the borrow output of the half subtractor and the second term is the inverted difference output of first X-OR.

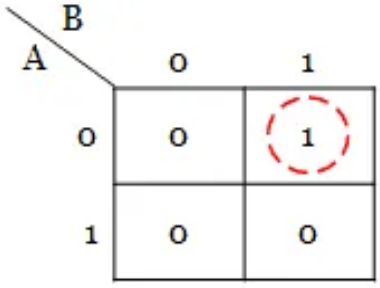
HALF SUBTRACTOR

TRUTH TABLE:

A	B	BORROW	DIFFERENCE
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

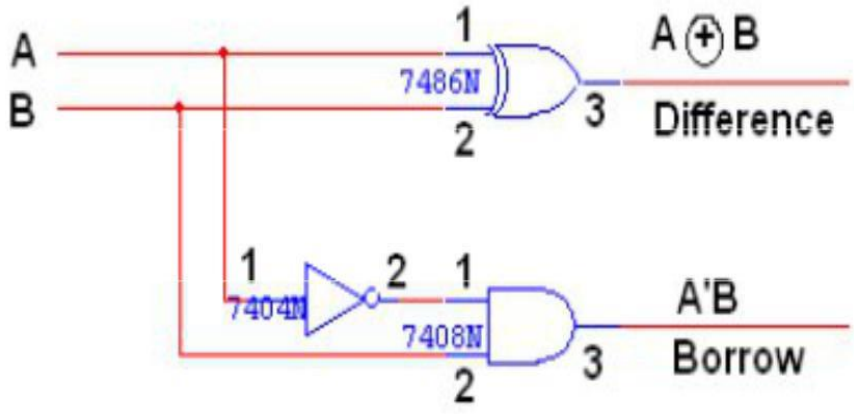


Difference = $A\overline{B} + \overline{A}B = A \oplus B$



Borrow = $\overline{A}B$

LOGIC DIAGRAM:



FULL SUBTRACTOR

TRUTH TABLE:

A	B	C	BORROW	DIFFERENCE
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-Map for Difference:

A \ BC	00	01	11	10
0		1		1
1	1		1	

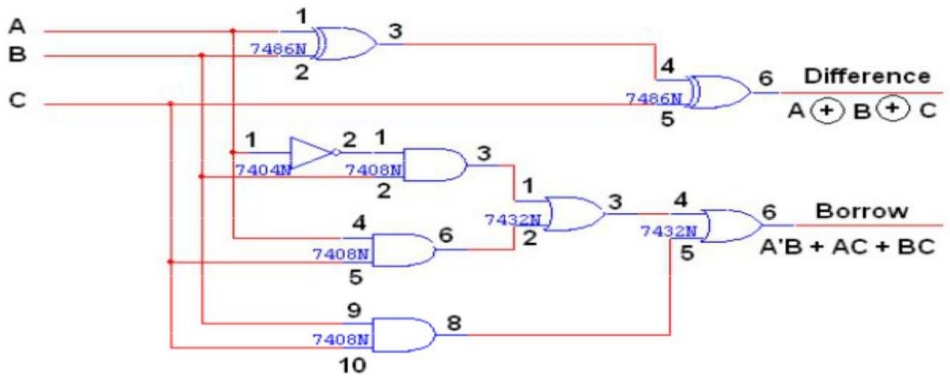
Difference = A'B'C + A'BC' + AB'C' + ABC

K-Map for Borrow:

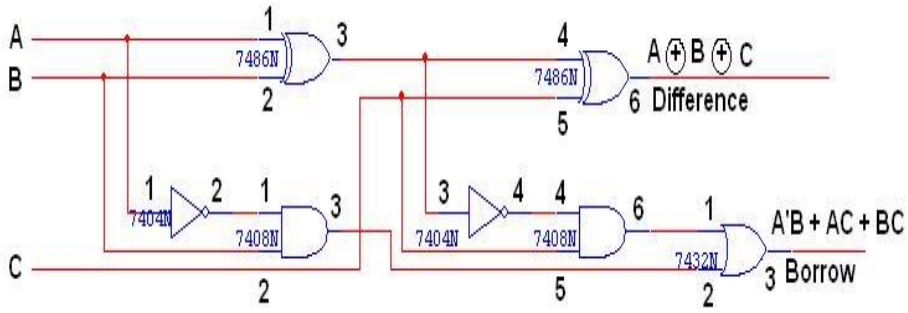
A \ BC	00	01	11	10
0		1	1	1
1			1	

Borrow = A'B + BC + A'C

LOGIC DIAGRAM:



FULL SUBTRACTOR USING TWO HALF SUBTRACTOR:



PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board.
3. Connect the inputs to the input switches provided in the Bread board.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions of LEDs.
6. Similarly follow these steps for other gates

PRECAUTIONS:

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.

5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

6. Take care while removing and inserting the IC on bread board.

RESULT:

Thus the half subtractor and full subtractor was designed and their truth table is verified.

6.Verification of the De-Morgan's Theorem.

NAME OF LABORATORY: Digital System Lab
LAB SUBJECT NAME/CODE: DCS /IT-305NAME OF DEPARTMENT: - E.C

Date of conduction: -

Date of submission: -

Submitted by other members: -

1. 2.

3. 4.

5. 6.

7. 8.

Group no: -

Signature

Name of faculty in charge:

Name of Technical Assistant:

OBJECT:

De-Morgan's developed a theorem that allows conversion between logic expressions that has inversions on the output to a different logic expression with the inversions on each of the inputs. This may allow for the simplification of a Boolean Expression by the cancellation of some redundant inversions. There are two Boolean Equations that represent De Morgan's Theorem:

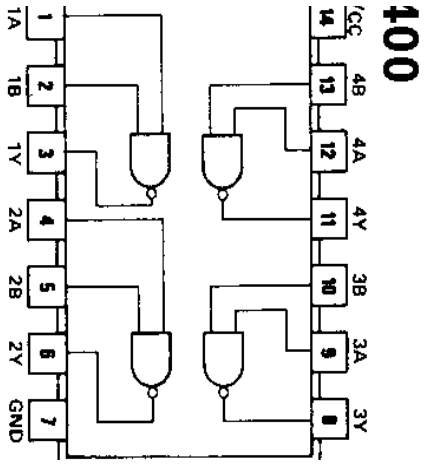
APPARATUS REQUIRED:

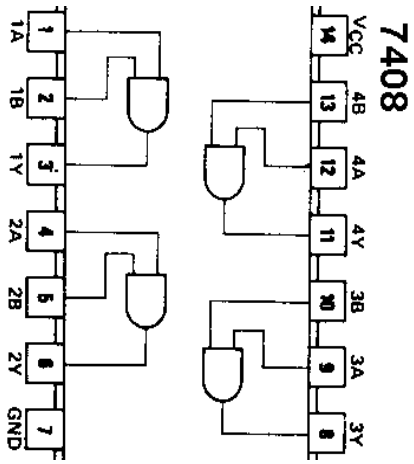
S.No.	COMPONENT	SPECIFICATION	QTY
	NAND GATE	IC 7400	
	NOT GATE	IC 7404	
	AND GATE	IC 7408	
	OR GATE	IC 7432	
	IC TRAINER KIT	-	
	WIRES	As Required	

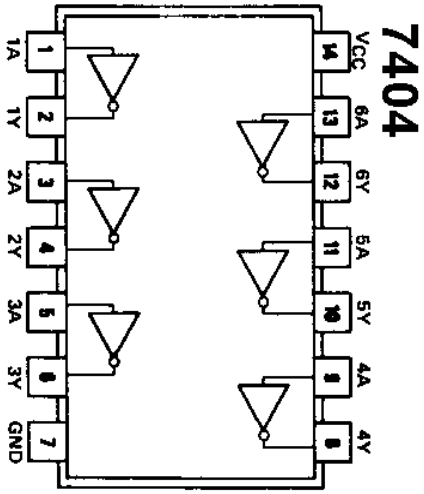
THEORY:

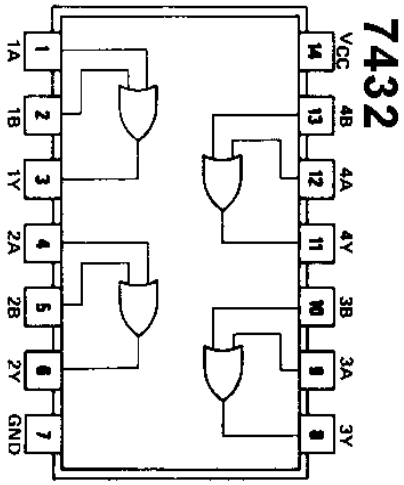
Generally you'll find that the basic logic functions AND, OR, NAND, NOR, and NOT are not sufficient to implement complex digital logic functions. These gates are the basis for building more complex logic circuits that are constructed using various combinations of gates which is known as Combinational Logic. Combinational logic requires the use of two or more gates to form a useful, complex function.

PIN DIAGRAM:



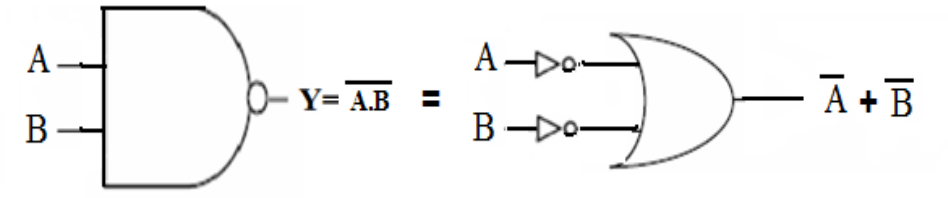






DE MORGAN`S THEOREM

1. $\overline{AB} = \overline{A} + \overline{B}$ ..... (I)



NAND Gate **Bubbled OR Gate**

FIG: a. Law 1

2. $\overline{A} + \overline{B} = \overline{A.B}$ ……. (II)

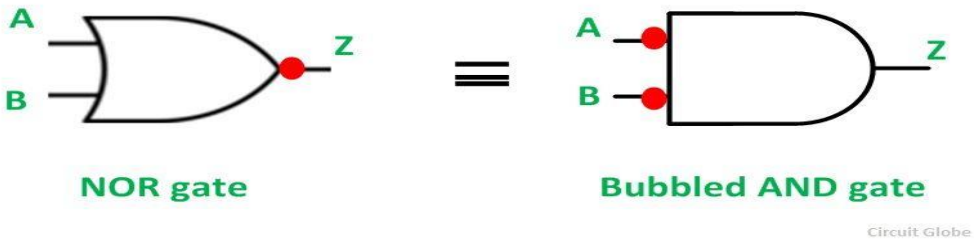


FIG: b. Law 2

3.A , B = ($\bar{A} + \bar{B}$)----------(III)

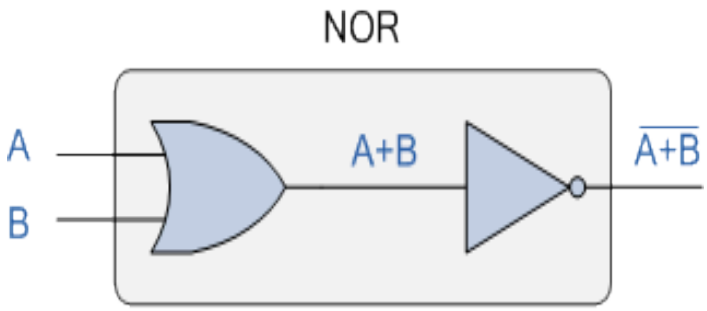


FIG: C. Law 3

4. A, B = $\bar{A}.\bar{B}$ ----------(IV)

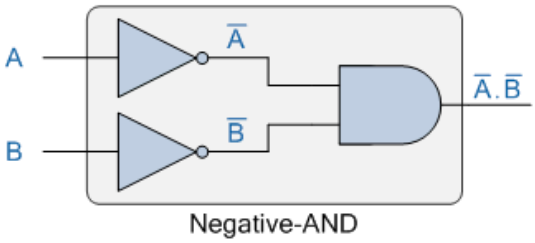


FIG: D. Law 4

PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board.
3. Connect the inputs to the input switches provided in the Bread board.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions of LEDs.
6. Similarly follow these steps for other gates

PRECAUTIONS:

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.
5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
6. Take care while removing and inserting the IC on bread board.

RESULT:

Thus the half subtractor and full subtractor was designed and their truth table is verified.

7. Study of S-R, J-K, T & D flip-flops.

NAME OF LABORATORY: Digital System Lab
LAB SUBJECT NAME/CODE: DCS /IT-305NAME OF DEPARTMENT: - E.C

Date of conduction:

Date of submission:

Submitted by other members:

1.	2.
3.	4.
5.	6.
7.	8.

Group no:

Signature

Name of faculty in charge:

Name of Technical Assistant:

OBJECT:-Study of S-R, J-K, T & D flip-flops.

APPARATUS REQUIRED: -

S.No.	COMPONENT	SPECIFICATION	QTY
	NAND GATE	IC 7400	
	NOT GATE	IC 7404	
	AND GATE	IC 7408	
	NOR GATE	IC 7402	
	IC TRAINER KIT	-	
	WIRES	As Required	

THEORY:

Logic circuits that incorporate memory cells are called sequential logic circuits; their output depends not only upon the present value of the input but also upon the previous values. Sequential logic circuits often require a timing generator (a clock) for their operation. The latch (flip-flop) is a basic bi-stable memory element widely used in sequential logic circuits. Usually there are two outputs, Q and its complementary value. Some of the most widely used latches are listed below.

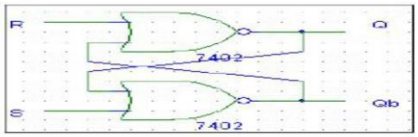
S-R LATCH:

An S-R latch consists of two cross-coupled NOR gates. An S-R flip-flop can also be design using cross-coupled NAND gates as shown. The truth tables of the circuits are shown below. A clocked S-R flip-flop has an additional clock input so that the S and R inputs are active only when the clock is high. When the clock goes low, the state of flip-flop is latched and cannot change until the clock goes high again. Therefore, the clocked S-R flip-flop is also called "enabled" S-R flip-flop.

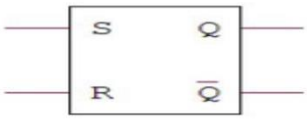
A D latch combines the S and R inputs of an S-R latch into one input by adding an inverter. When the clock is high, the output follows the D input, and when the clock goes low, the state is latched.

A S-R flip-flop can be converted to T-flip flop by connecting S input to Qb and R to Q.

S-R LATCH:



(A) LOGIC DIAGRAM

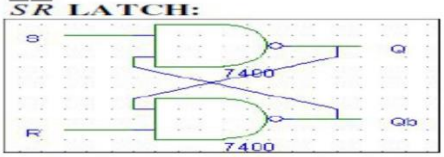


(B) SYMBOL

TRUTH TABLE

S	R	Q+	$\overline{Q}$b+
0	0	Q	$\overline{Q}$b
0	1	0	1
1	0	1	0
1	1	0*	0*

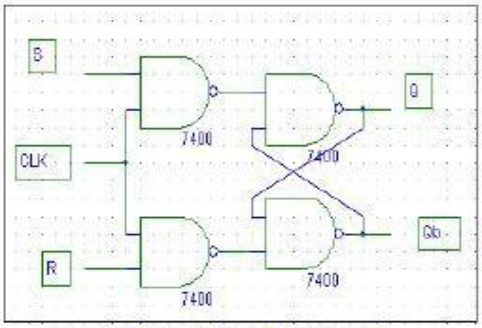
$\overline{S}\overline{R}$ LATCH:



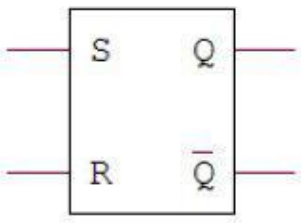
TRUTH TABLE

S	R	Q+	$\overline{Q}$b+
0	0	1*	1*
0	1	1	0
1	0	0	1
1	1	Q	$\overline{Q}$b

CIRCUIT DIAGRAM:



(A) LOGIC DIAGRAM



(B) SYMBOL

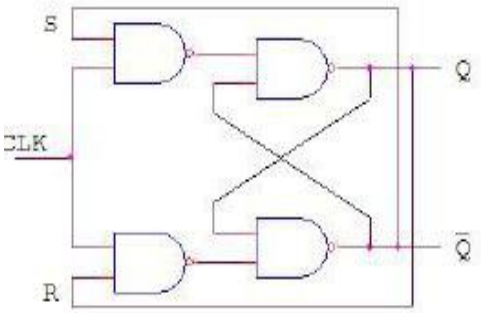
1. S-R FLIP FLOP :

TRUTH TABLE

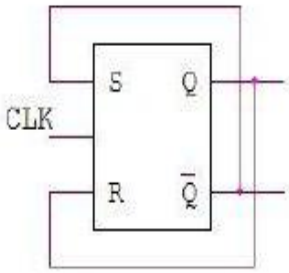
S	R	Q+	$\overline{Q}$b+
0	0	Q	$\overline{Q}$b
0	1	0	1
1	0	1	0
1	1	0*	0*

2. CONVERSION OF SR-FLIP FLOP TO T-FLIP FLOP (TOGGLE):

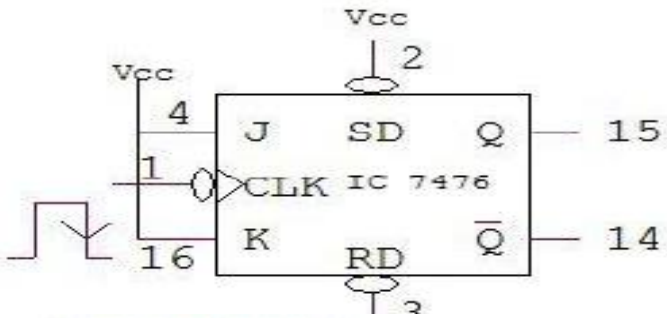
LOGIC DIAGRAM



SYMBOL



T FLIP FLOP USING IC 7476

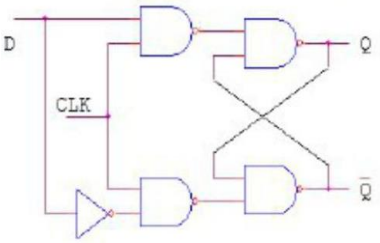


TRUTH TABLE

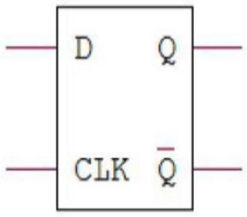
T	Qn + 1
0	Qn
1	$\overline{Qn}$

3. CONVERSION OF SR-FLIP FLOP TO D-FLIP FLOP :

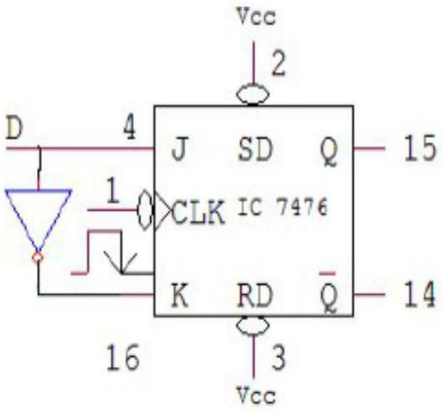
LOGIC DIAGRAM



SYMBOL



D FLIP FLOP USING IC 7476

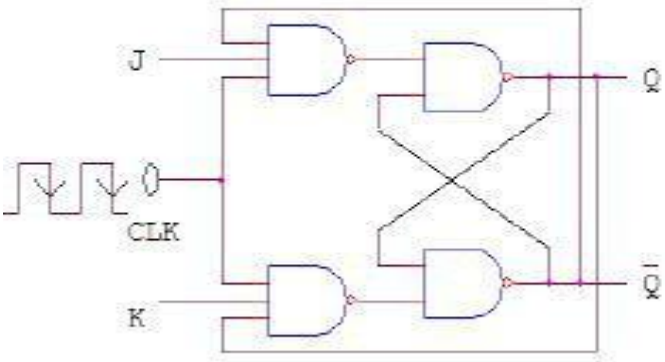


TRUTH TABLE

CLOCK	D	Q+	$\overline{Q+}$
0	X	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

4. CONVERSION OF SR-FLIP FLOP TO JK-FLIP FLOP:

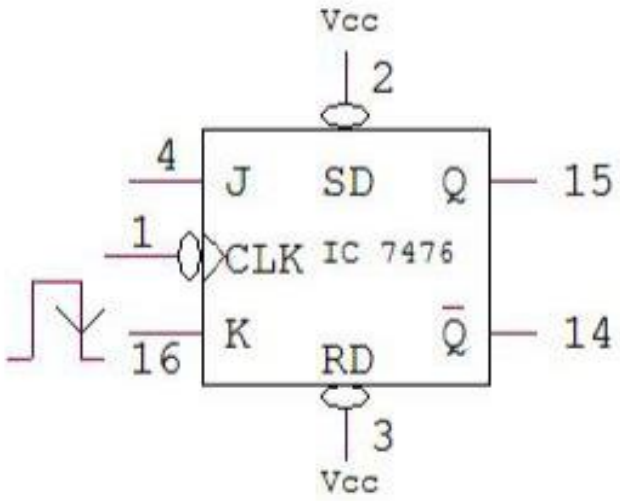
LOGIC DIAGRAM



TRUTH TABLE

Clock	J	K	Q+	Q'+	Comment
1	0	0	Q	Q'	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q'	Q	Toggle

LOGIC DIAGRAM



TRUTH TABLE

SD	RD	Clock	J	K	Q	Q'	Comment
0	0	Not Allowed					
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	1	0	0	NC	NC	Memory
1	1	1	0	1	0	1	Reset
1	1	1	1	0	1	0	Set
1	1	1	1	1	Q'	Q	Toggle

PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board.
3. Connect the inputs to the input switches provided in the Bread board.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions LEDs.
6. Similarly follow these steps for other gates.

PRECAUTIONS:

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.
5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
6. Take care while removing and inserting the IC on bread board.

RESULT:

Truth tables of all the Flip Flops are Verifird.

8.Study of Multiplexer

NAME OF LABORATORY: Digital System Lab
LAB SUBJECT NAME/CODE: DCS/IT-305 NAME OF DEPARTMENT: - E.C

Date of conduction: -

Date of submission: -

Submitted by other members: -

1. 2.

3. 4.

5. 6.

7. 8.

Group no: -

Signature

Name of faculty in charge:

Name of Technical Assistant:

OBJECT:-Multiplexer based boolean function realization.

APPARATUS REQUIRED:

S.No.	COMPONENT	SPECIFICATION	QTY
	NOT GATE	IC 7404	
	3 i/p AND GATE	IC 7411	
	OR GATE	IC 7432	
	IC TRAINER KIT	-	
	WIRES	As Required	

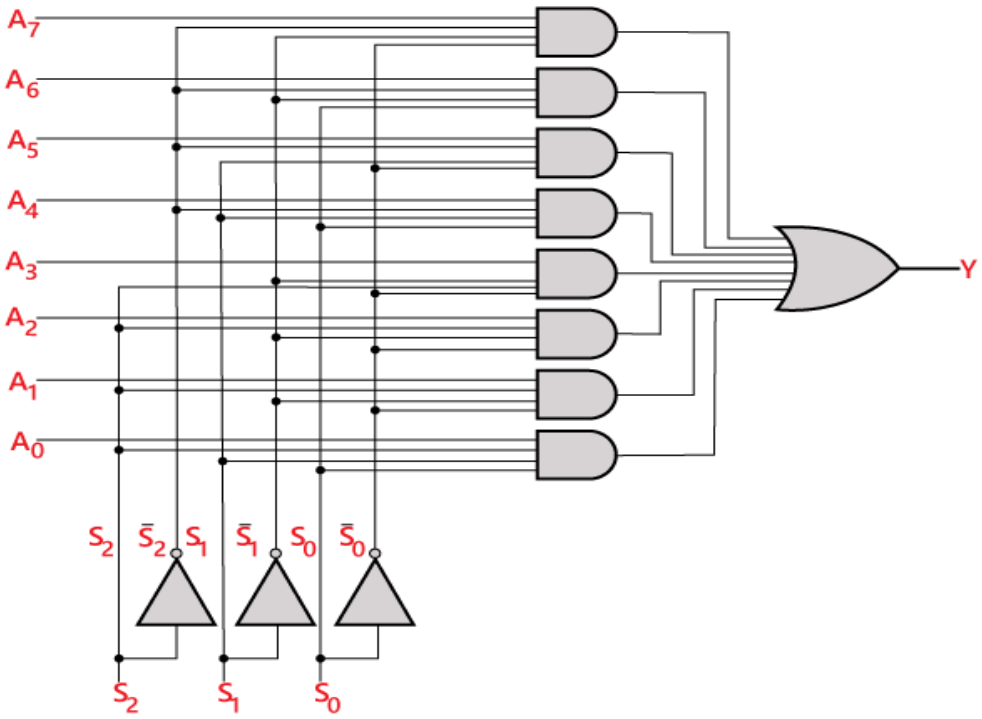
THEORY:

MULTIPLEXER:

Multiplexer means transmitting a large number of information units over asmaller number of channels or lines. A digital multiplexer is a combinational circuit that se lects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2n input line and n selection lines whose bit combination determine which input is selected.

BLOCK DIAGRAM:

CIRCUIT DIAGRAM FOR MULTIPLEXER:



TRUTH TABLE:

INPUTS			Output
S_2	S_1	S_0	Y
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board.
3. Connect the inputs to the input switches provided in the Bread board.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions LEDs.
6. Similarly follow these steps for other gates.

PRECAUTIONS:

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.
5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
6. Take care while removing and inserting the IC on bread board.

RESULT:

Thus the multiplexer and demultiplexer using logic gates was designed
IC 74150 and IC 74154 also studied.

9.Study of De-Multiplexer

NAME OF LABORATORY: Digital System Lab
LAB SUBJECT NAME/CODE: DCS/IT-305 NAME OF DEPARTMENT: - E.C

Date of conduction:

Date of submission:

Submitted by other members:

1.	2.
3.	4.
5.	6.
7.	8.

Group no:

Signature

Name of faculty in charge:

Name of Technical Assistant:

OBJECT:-De-Multiplexer based boolean function realization.

APPARATUS REQUIRED:

S.No.	COMPONENT	SPECIFICATION	QTY
	NOT GATE	IC 7404	
	3 i/p AND GATE	IC 7411	
	OR GATE	IC 7432	
	IC TRAINER KIT	-	
	WIRES	As Required	

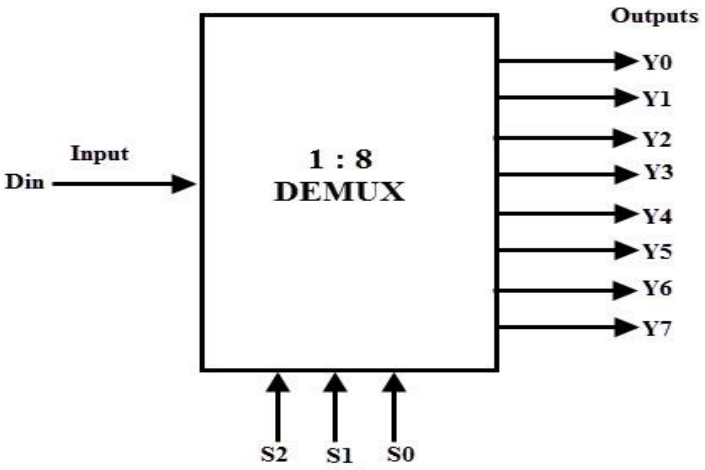
THEORY:

DEMULTIPLEXER:

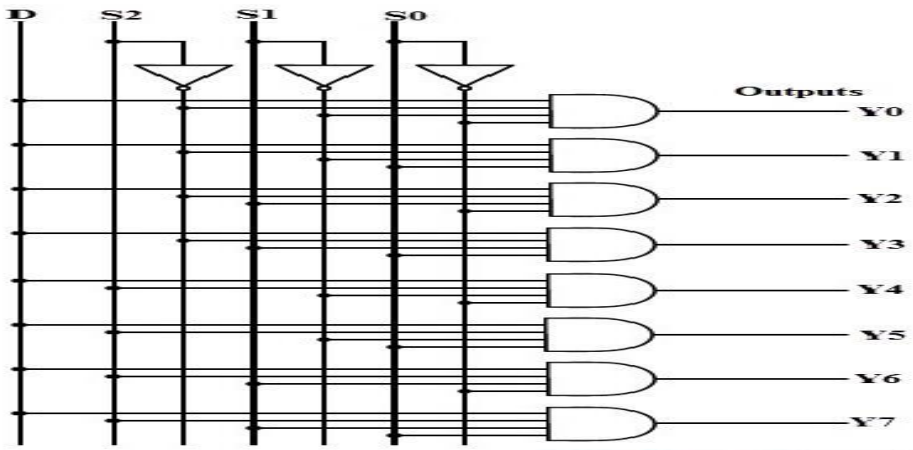
The function of De-multiplexer is in contrast to multiplexer function. It takes informationfrom one line and distributes it to a given number of output lines. For this reason the de-multiplexer is also known as a data distributor. Decoder can

also be used as de-multiplexer. In the 1: 4 de-multiplexer circuit, t he data input line goes to a ll of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

BLOCK DIAGRAM:



LOGIC DIAGRAM FOR DEMULTIPLEXER:



TRUTH TABLE:

Data Input	Select Inputs			Outputs							
D	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board.
3. Connect the inputs to the input switches provided in the Bread board.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions of LEDs.
6. Similarly follow these steps for other gates.

PRECAUTIONS:

1. Connections must be tight on the bread board.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.
5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
6. Take care while removing and inserting the IC on bread board.

RESULT:

Thus the multiplexer and demultiplexer using logic gates was designed
IC 74150 and IC 74154 also studied.

10. Study of Asynchronous Counter

NAME OF LABORATORY: Digital System Lab
LAB SUBJECT NAME/CODE: DCS/IT-305 NAME OF DEPARTMENT: - E.C

Date of conduction:

Date of submission:

Submitted by other members:

1. 2.

3. 4.

5. 6.

7. 8.

Group no:

Signature

Name of faculty in charge:

Name of Technical Assistant:

OBJECT:-To Design Asynchronous Counter in Up and Down Mode

APPARATUS REQUIRED:

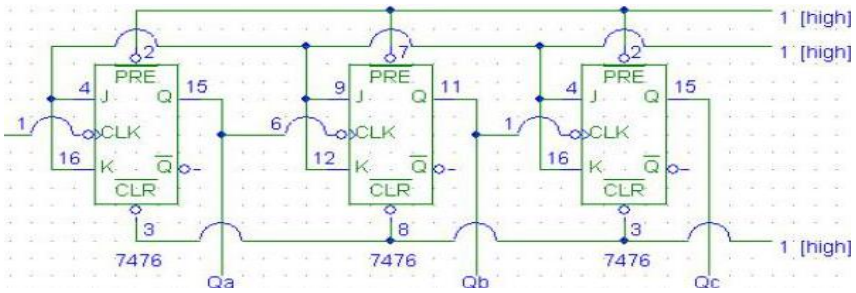
S.No.	COMPONENT	SPECIFICATION	QTY
	JK FLIP FLOP Dual	IC 7476	
	IC TRAINER KIT	--	
	WIRES	As Required	

THEORY:

A counter in which each flip-flop is triggered by the output goes to previous flip-flop. As all the flip-flops do not change state simultaneously spike occur at the output. To avoid this, strobe pulse is required. Because of the propagation delay the operating speed of asynchronous counter is low. Asynchronous counter are easy and simple to construct.

CIRCUIT DIAGRAM:

MOD-8 UP COUNTER:

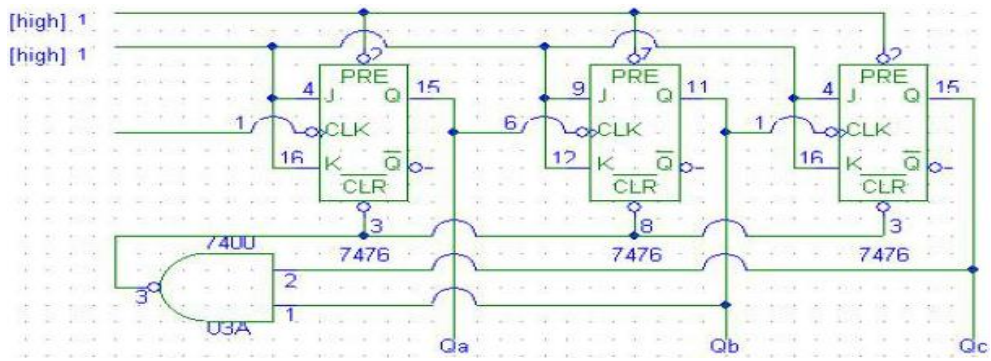


TRUTH TABLE

CLK	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

CIRCUIT DIAGRAM:

MOD_6 UP COUNTER:

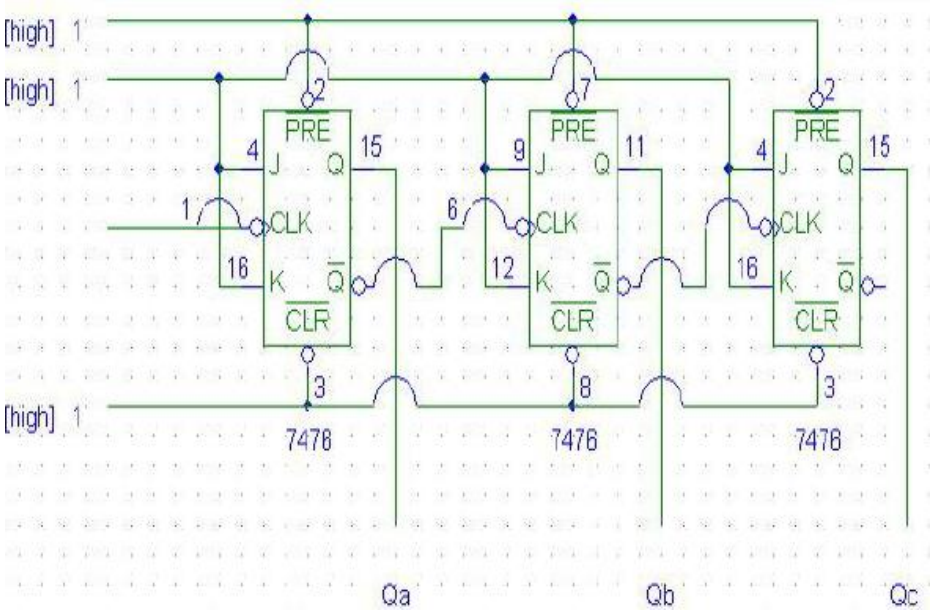


TRUTH TABLE

CLK	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	0	0	0

CIRCUIT DIAGRAM:

MOD_8 DOWN COUNTER:

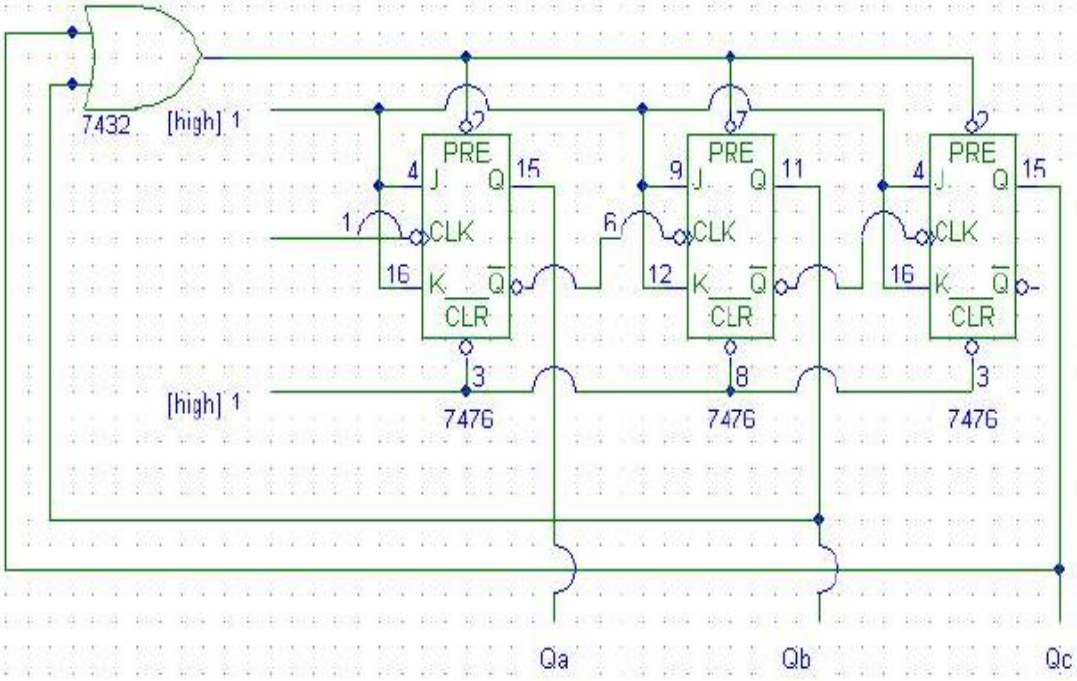


TRUTH TABLE

CLK	Q_C	Q_B	Q_A
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0
8	1	1	1

CIRCUIT DIAGRAM:

MOD_6 DOWN COUNTER:



TRUTH TABLE

CLK	Q_C	Q_B	Q_A
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	1	1	1

PROCEDURE:

1. Place the IC 74XXLS on the Bread board.
2. Connect VCC and ground to the respective pins on the Bread board/Trainer kit .
3. Connect the inputs to the input switches provided in the Bread board/Trainer kit.
4. Connect the outputs to the switches of output LEDs.
5. Apply various combinations of inputs as shown in the truth table and observe the conditions LEDs.
6. Similarly follow these steps for other gates.

PRECAUTIONS:

1. Connections must be tight on the bread board/Trainer kit.
2. Identify the pins of the IC properly.
3. Carefully connect VCC and ground to the respective pins on the Bread board.
4. Do not short any pin of IC.
5. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
6. Take care while removing and inserting the IC on bread board.

RESULT:

The working of Mod-N Asynchronous counters is verified.